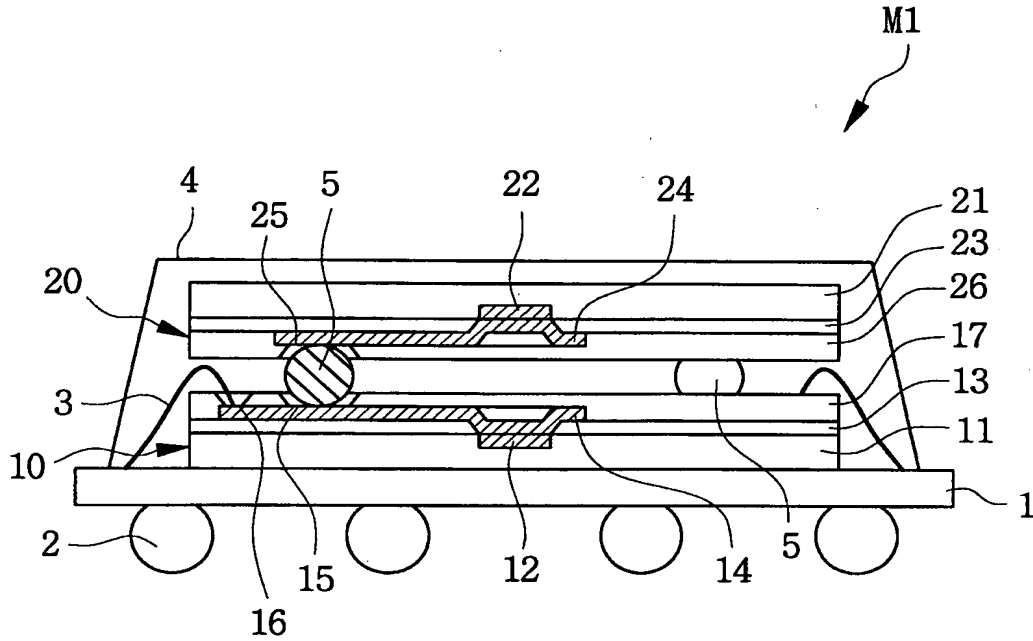


FIG. 1
(Prior Art)



The diagram shows a rectangular device 30 with a grid of vertical elements. A horizontal dashed line C1 passes through the middle. Vertical arrows A1 and A2 indicate a vertical axis. Horizontal arrows II indicate a horizontal axis. A dashed box T encloses a portion of the grid. Labels S, P, and G are placed at the intersections of the grid lines. On the right side, labels 35a, 35b, 35c, 39a, 39b, 39c, 36a, 36b, and 36c are grouped by brackets 35, 39, and 36 respectively. A label E1 points to a specific element at the bottom right.

FIG. 3B

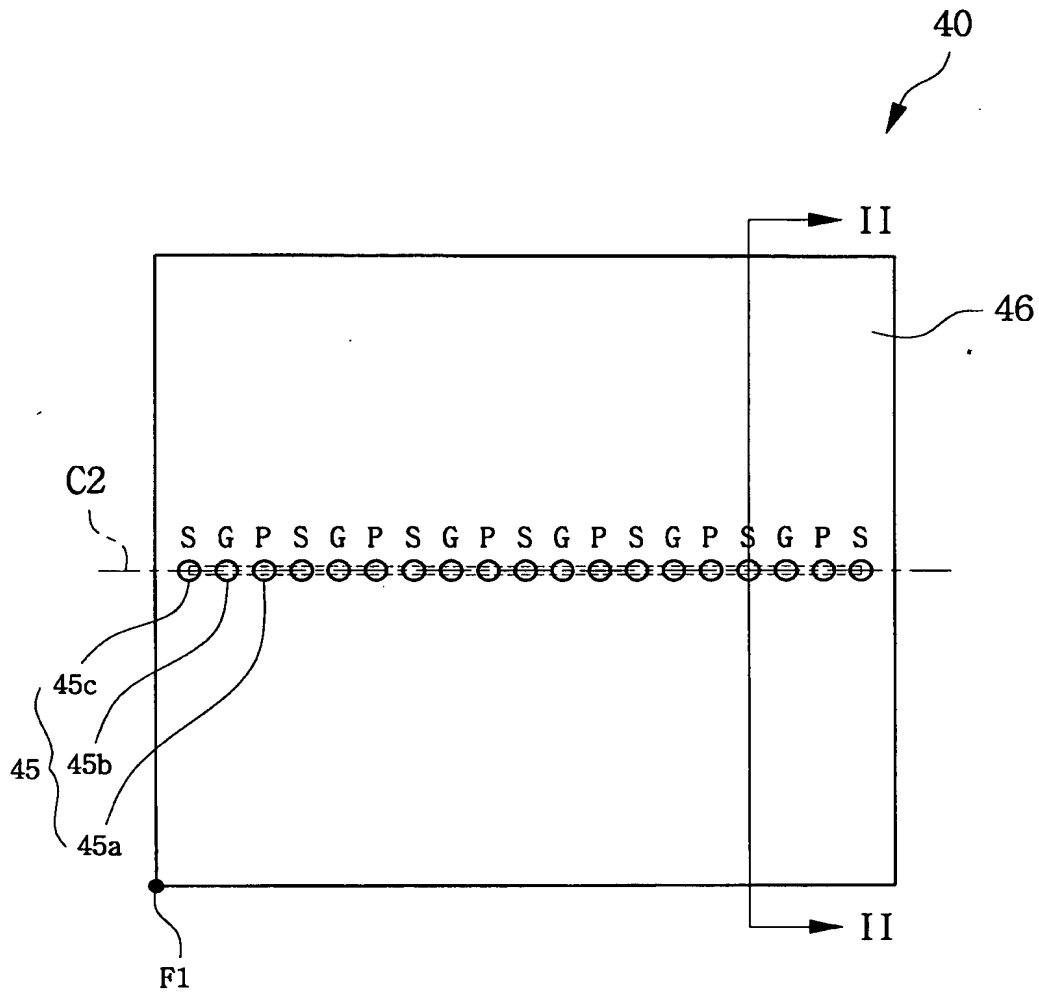


FIG. 3C

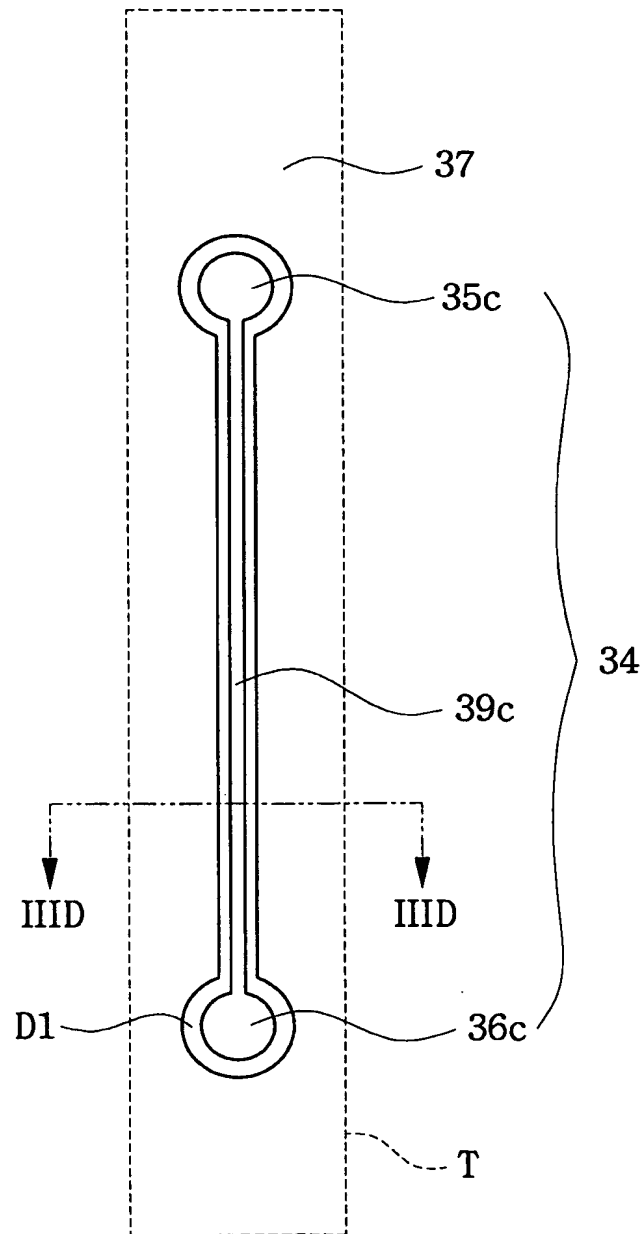
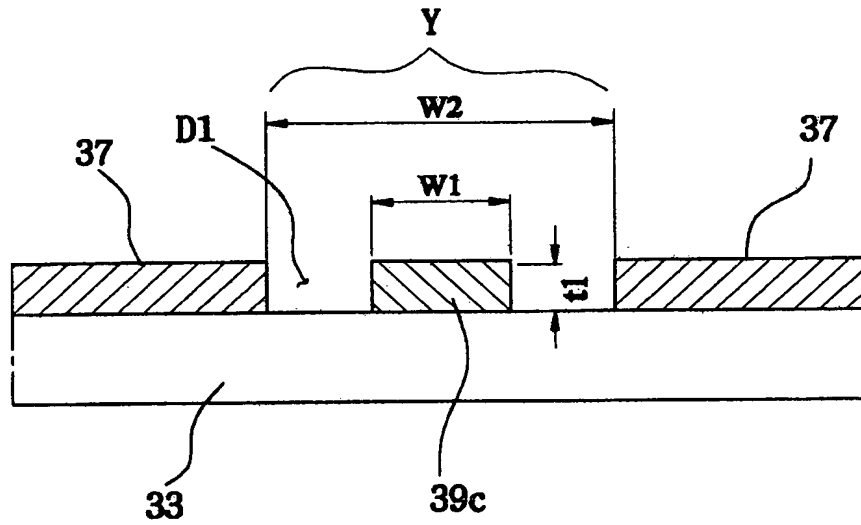


FIG. 3D



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FIG. 4

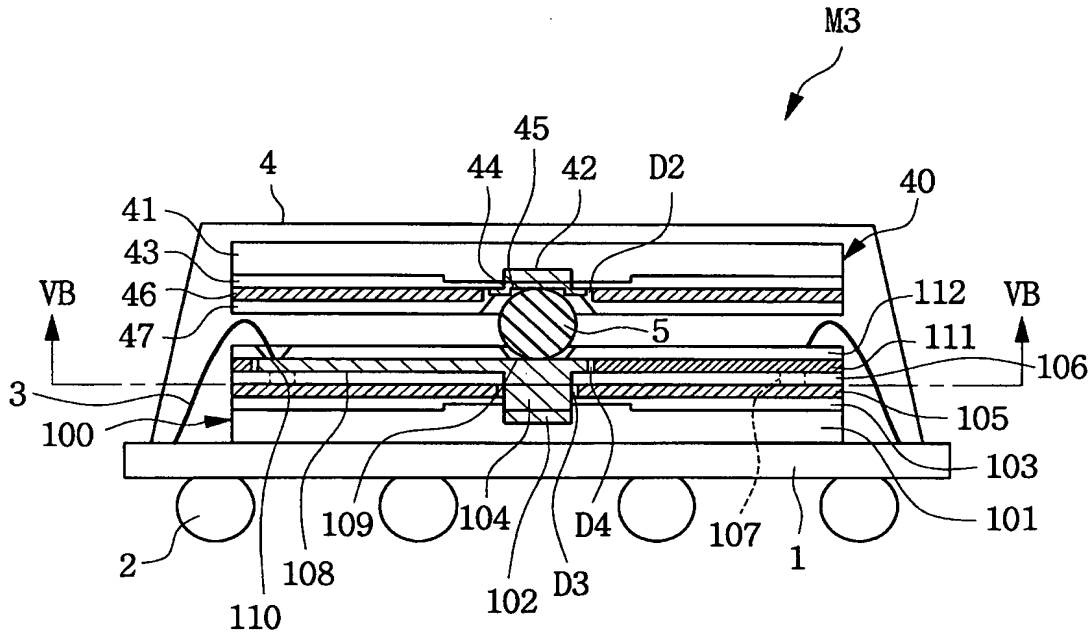


FIG. 6

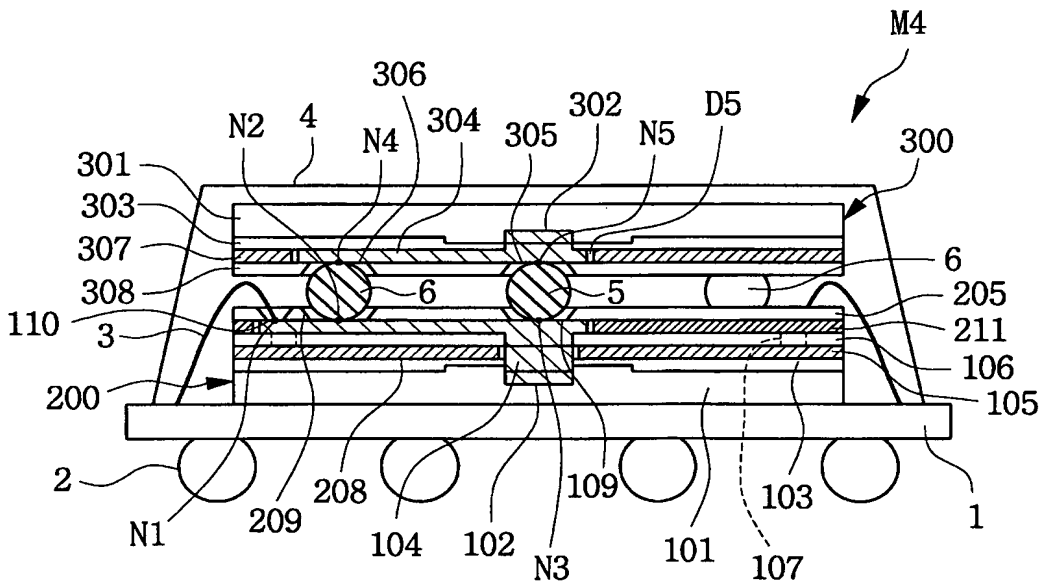
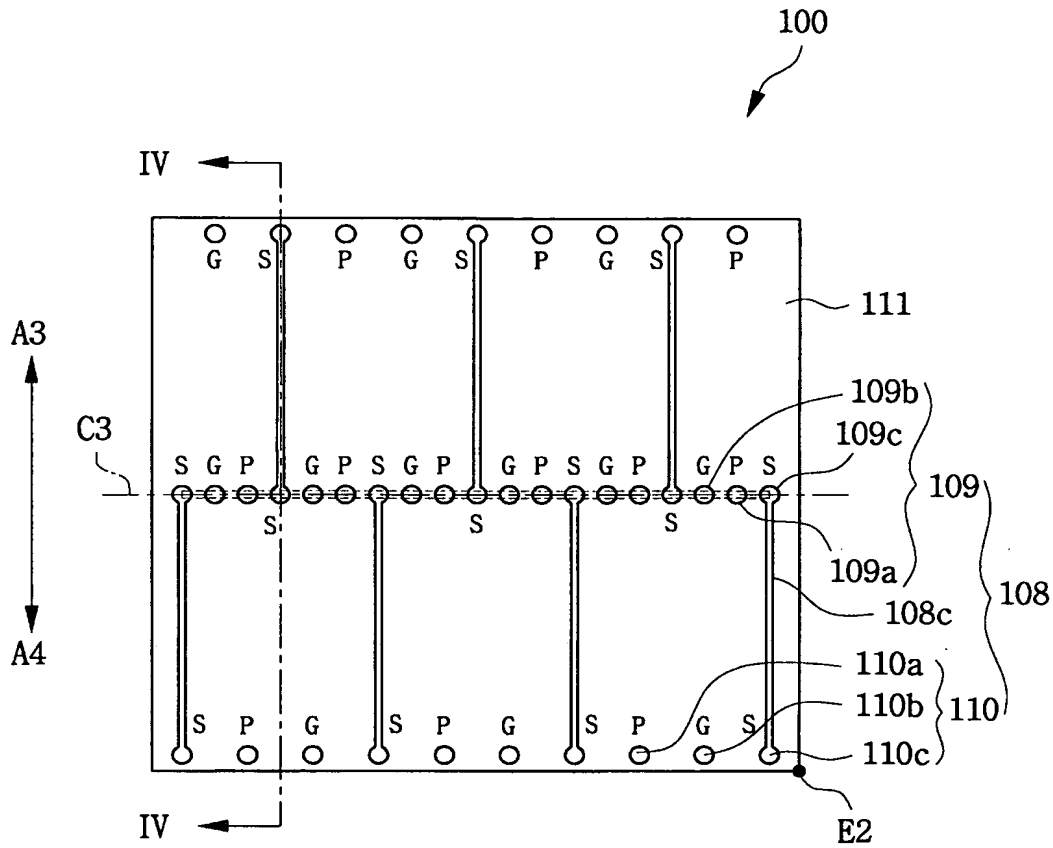


FIG. 5A



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FIG. 5B

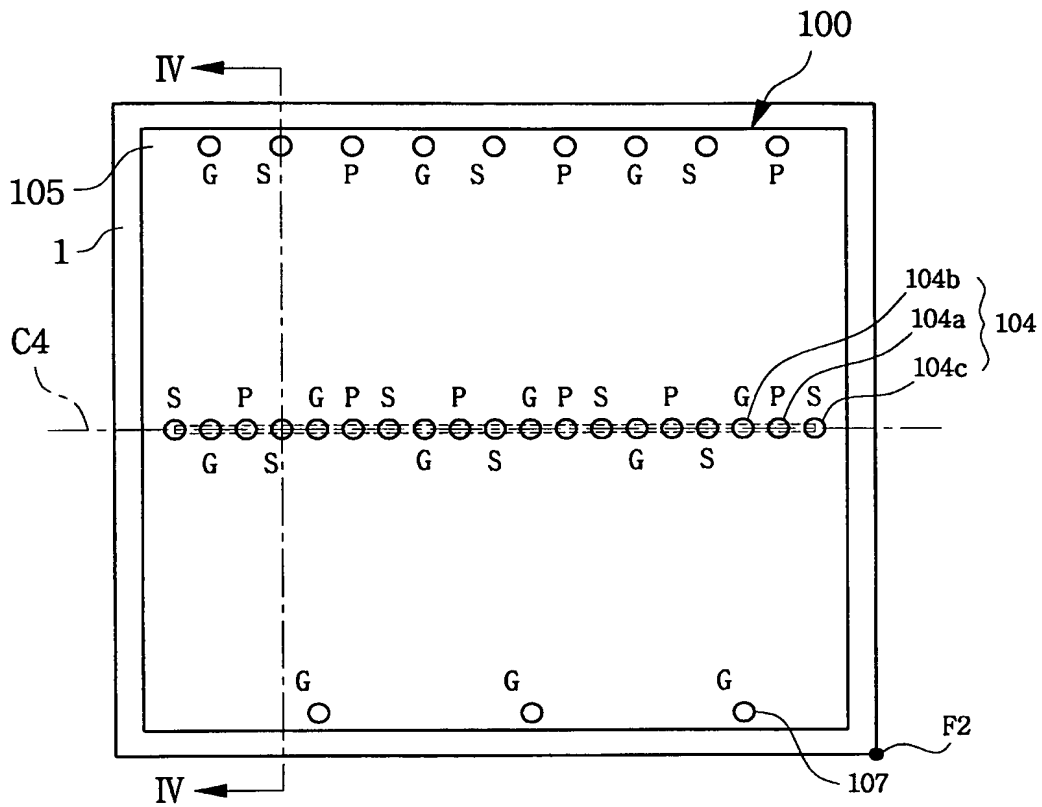
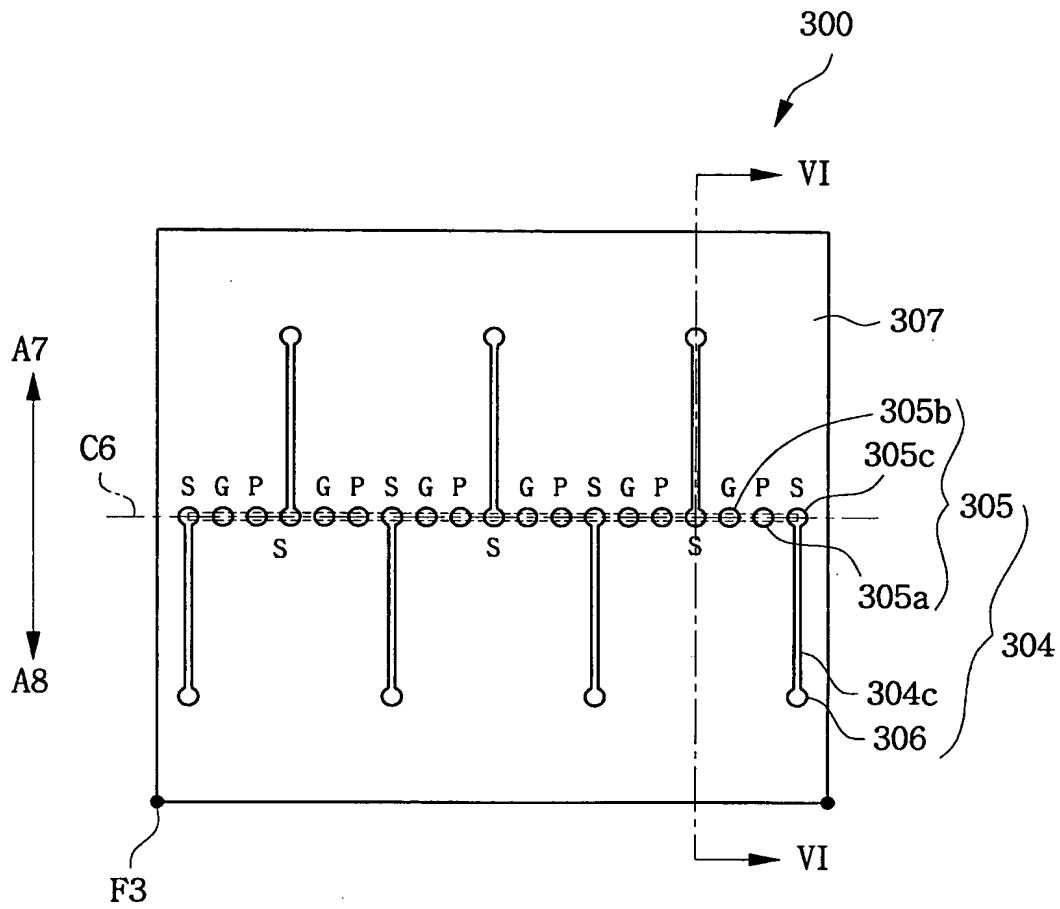


Diagram illustrating a plan view of a semiconductor device 200. The device features a grid of gates (G), source/drain regions (S), and polysilicon regions (P). The layout includes a central horizontal region 109, vertical regions 208, and a bottom region 110. A dashed line C5 and arrows A5/A6 indicate directions. Labels include 211, 109b, 109c, 109a, 208c, 209, 208d, 110c, 110b, 110a, and E3.

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FIG. 7B



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FIG. 8A

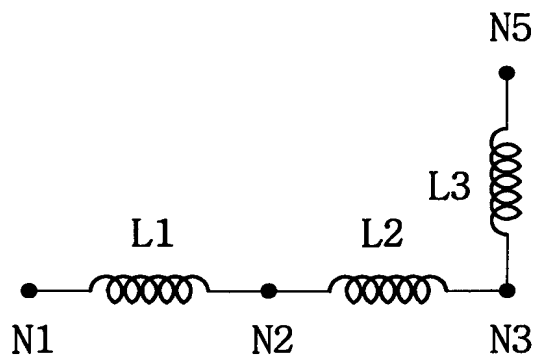
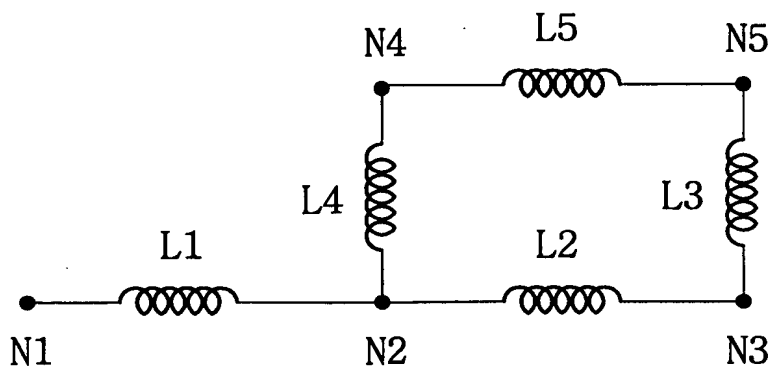


FIG. 8B



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FIG. 9A

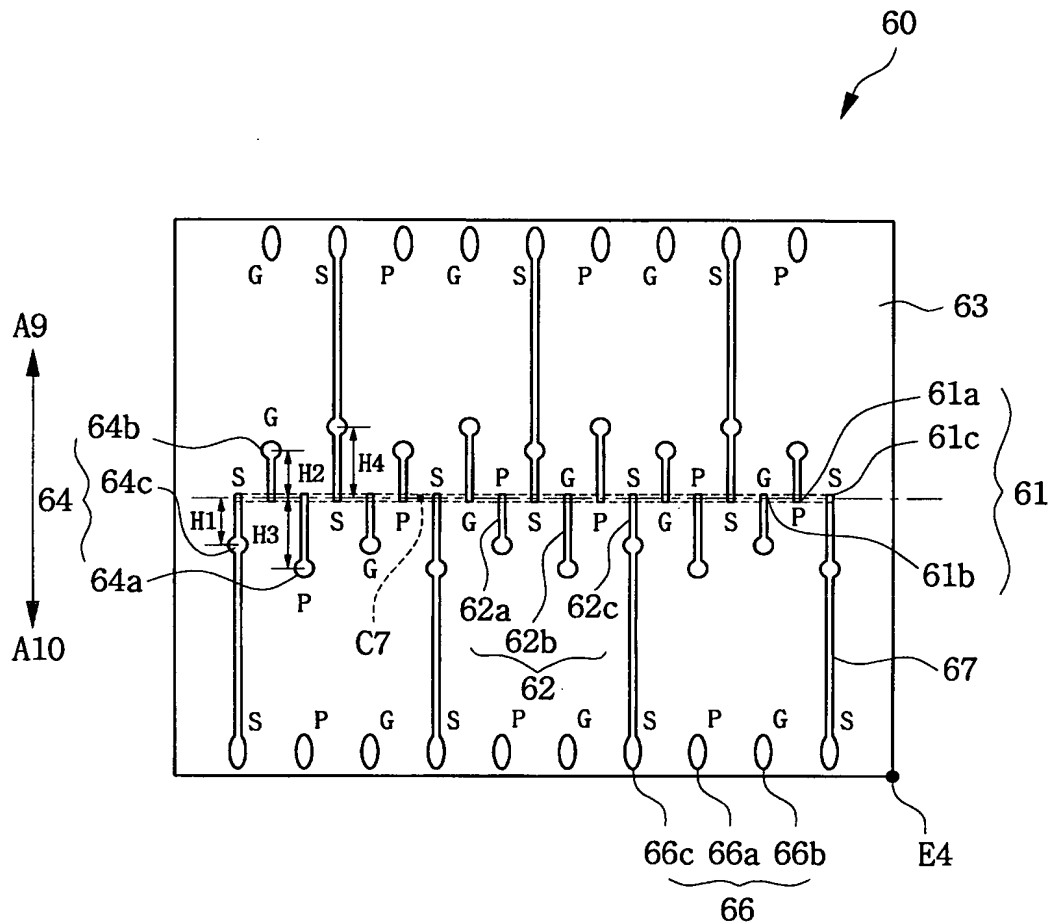
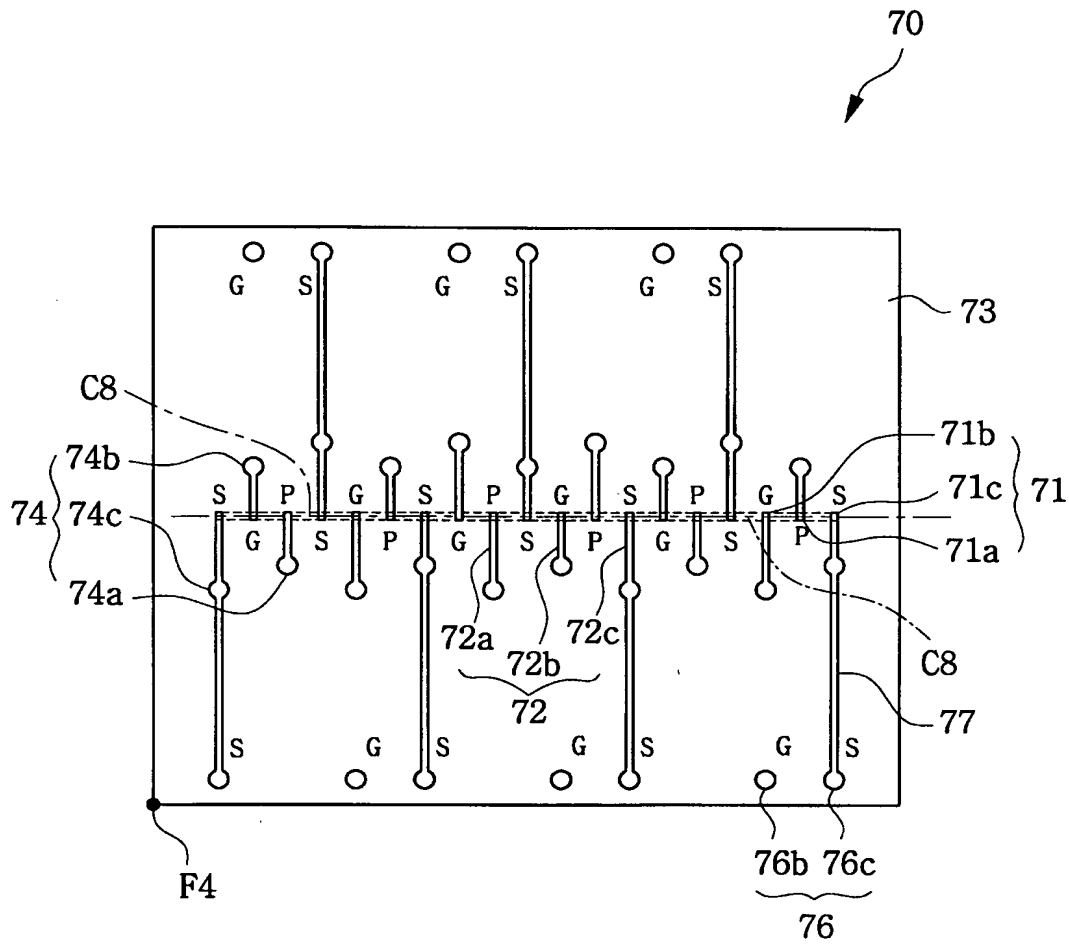


FIG. 9B



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FIG. 10A

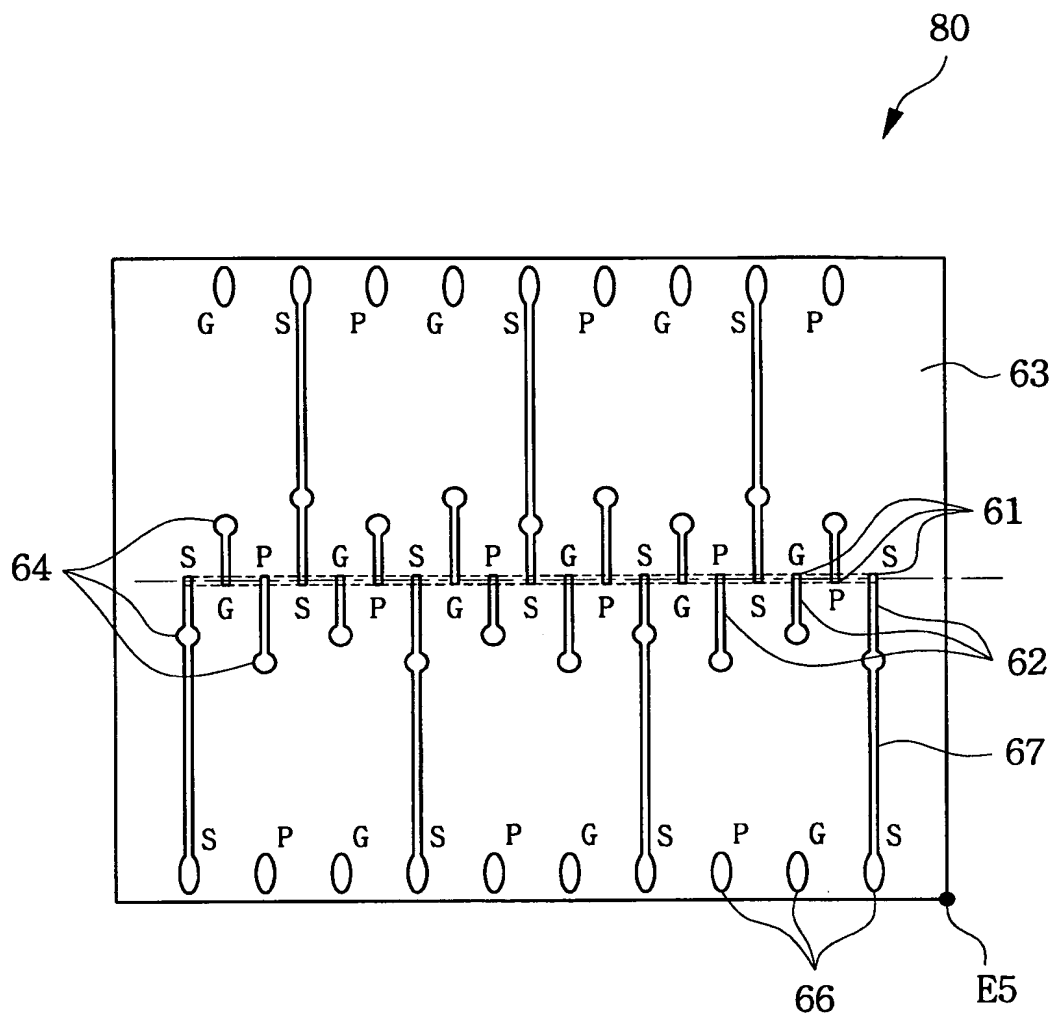
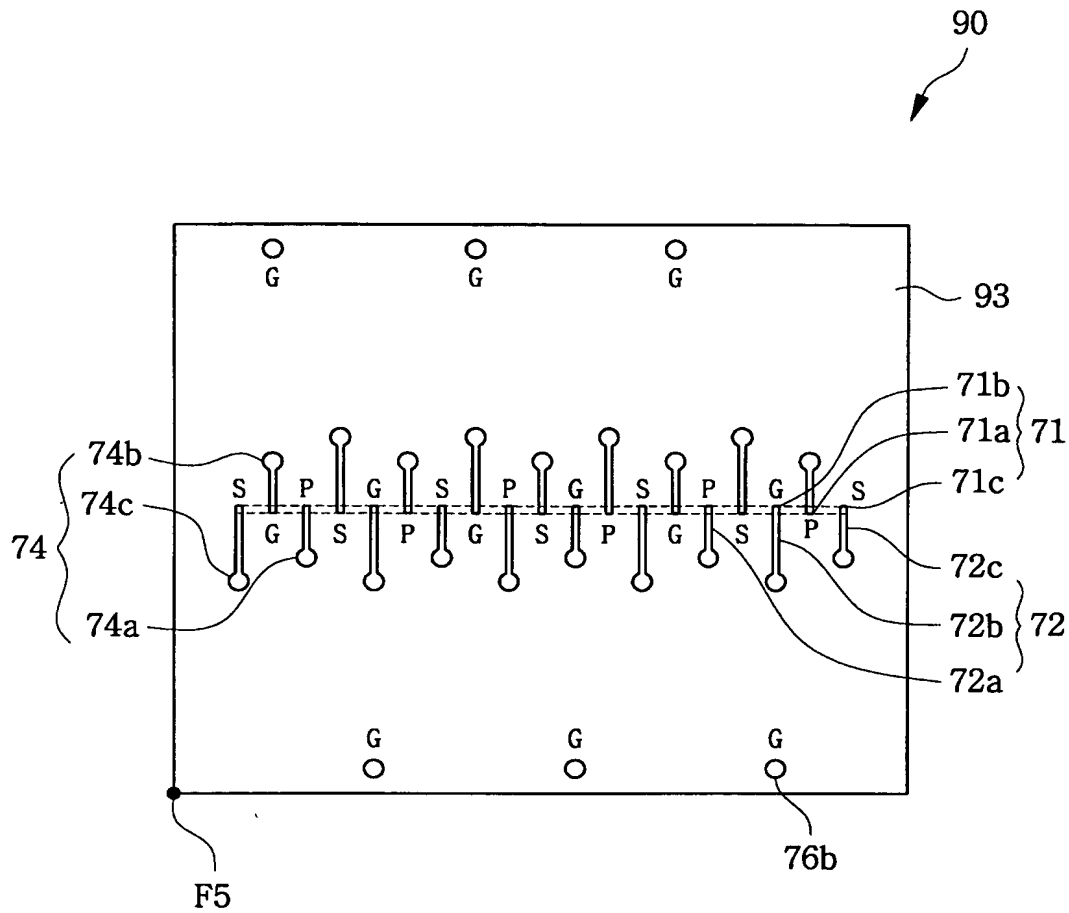


FIG. 10B



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FIG. 11A

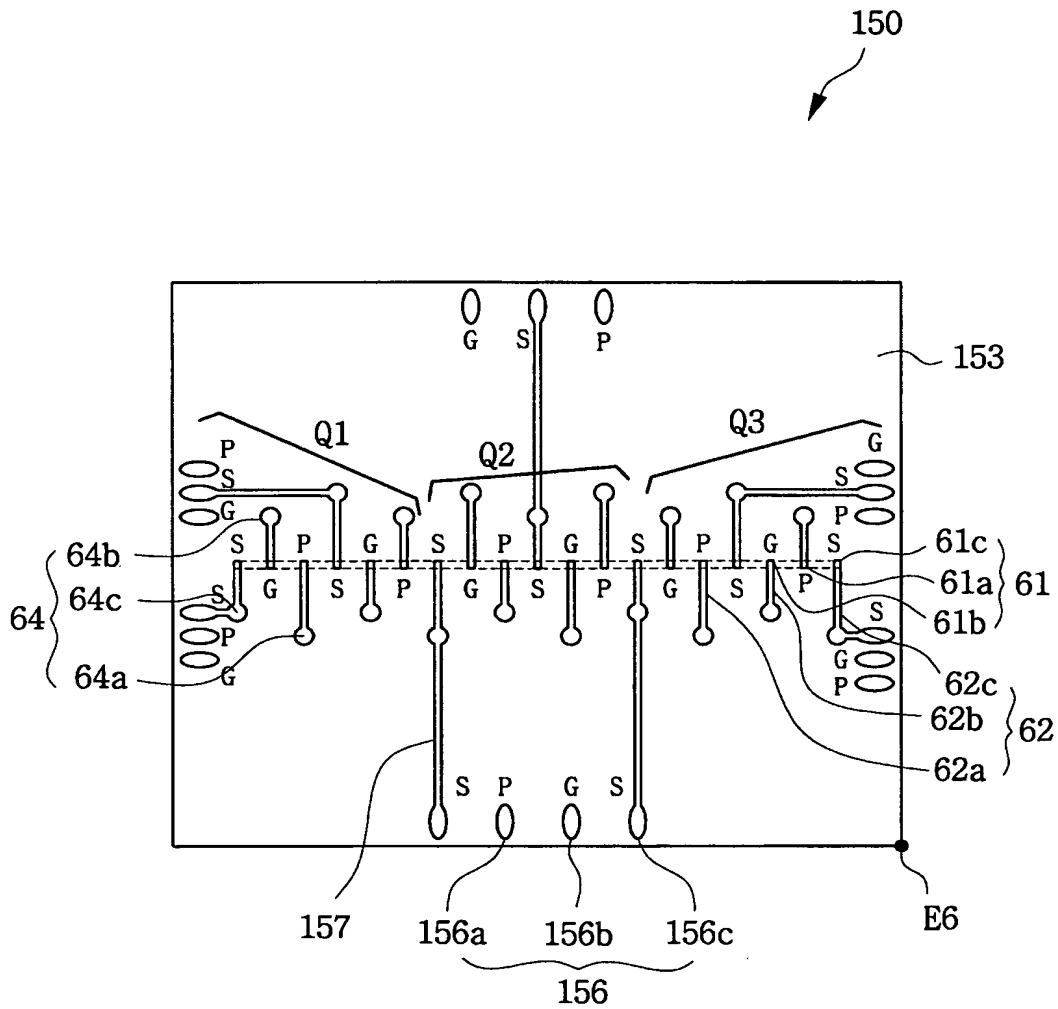
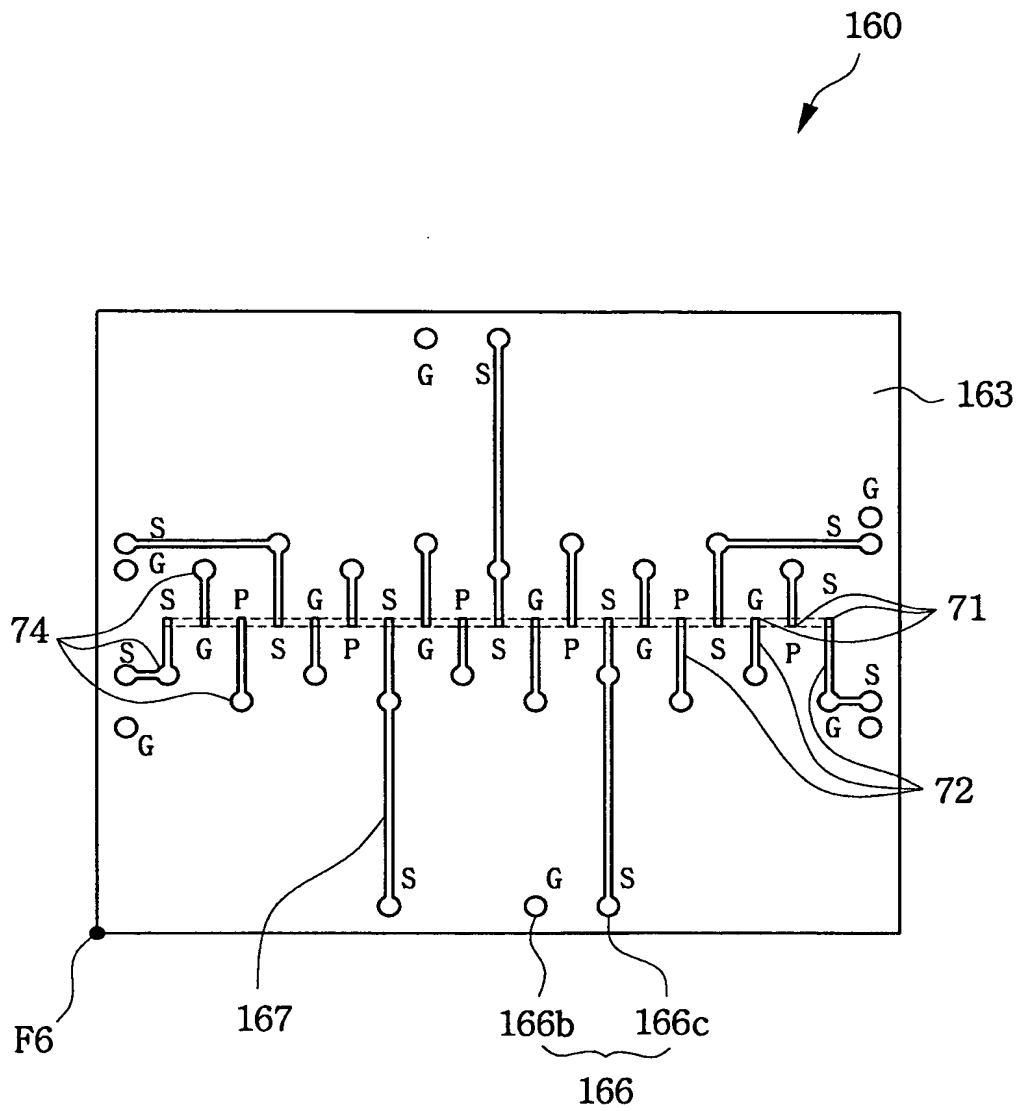


FIG. 11B



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FIG. 12A

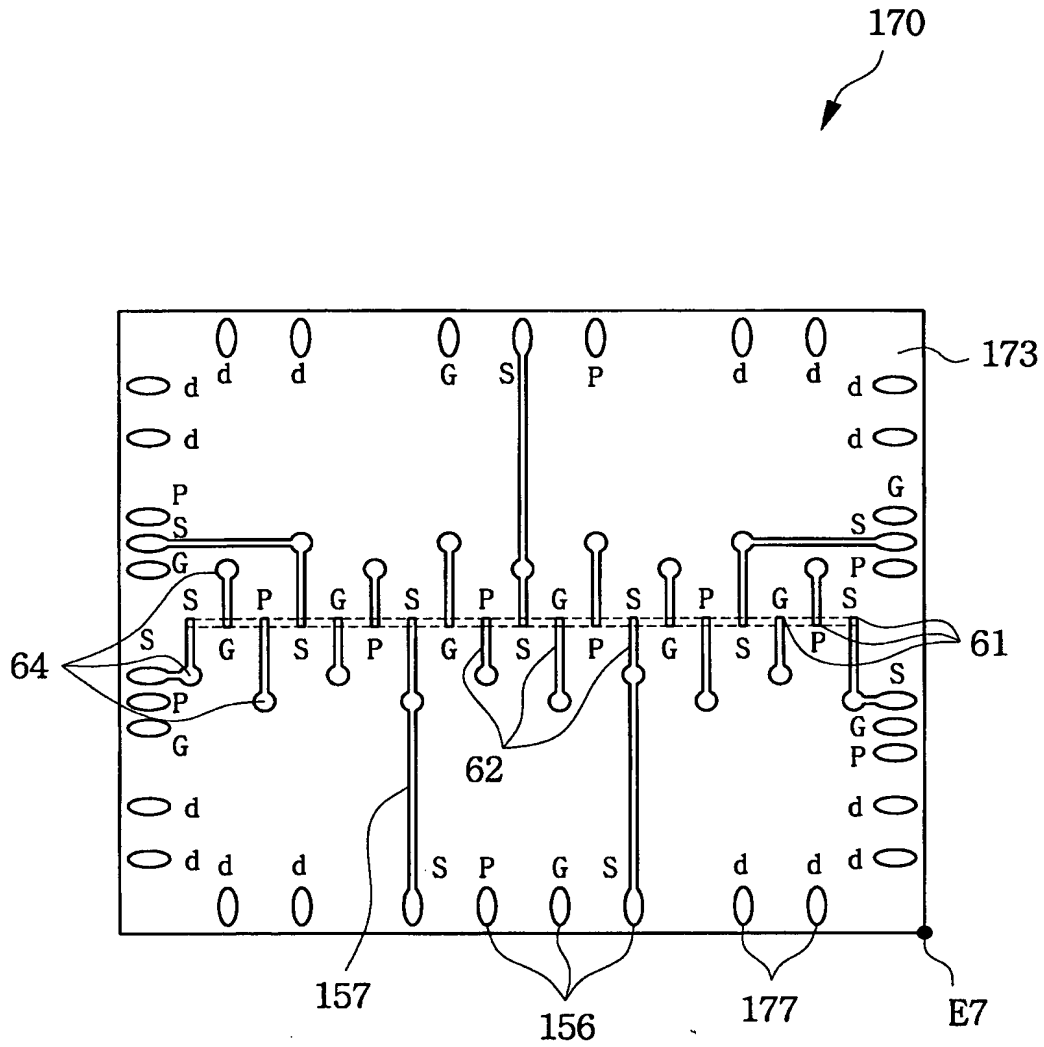


FIG. 12B

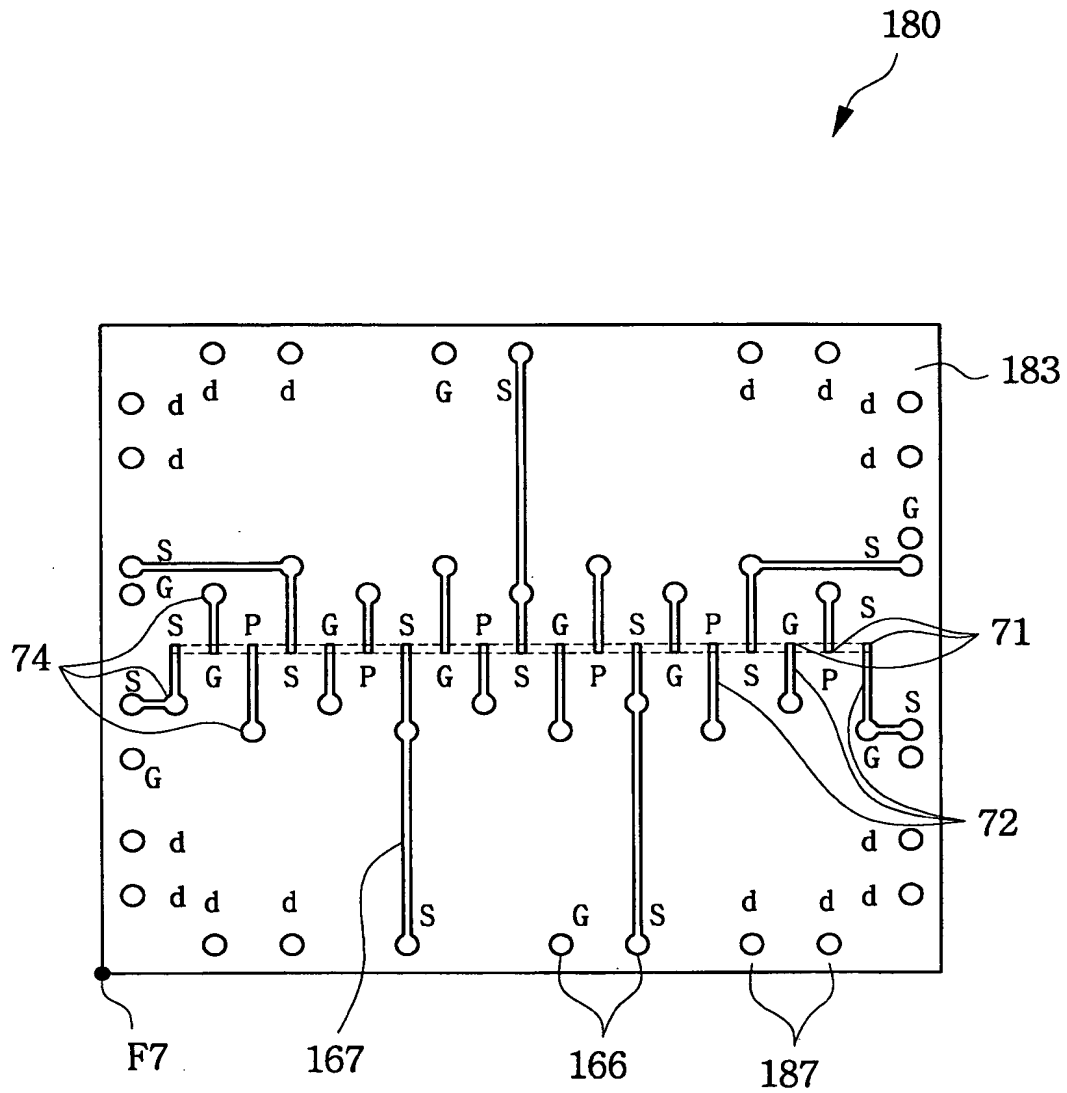


FIG. 13

